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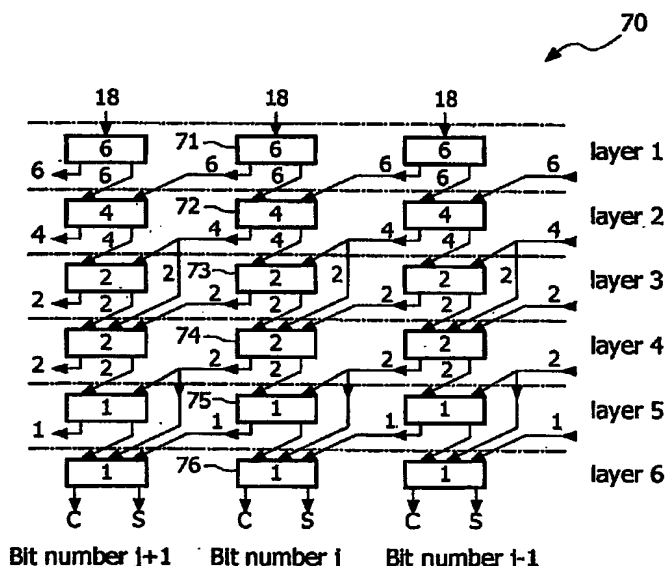
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(54) Title: **LONG-INTEGER MULTIPLIER**



(57) Abstract: An adder circuit for multiplying two long integers deploys a network of adders for summing a succession of words of the long integers to generate intermediate results. The number of addends varies as a function of bit position and the network of adders is designed to reduce the number of levels of adders in the network according to a maximum number of expected addends. A number of strategically placed extra adders may be positioned in the network to further reduce the number of levels. An output stage may be provided that adds sum and carry outputs of the network and retains a most significant bit for use with a subsequent calculation output of the network. The network may be configured so that a subsequent calculation by the network can commence before the previous calculation has been completed, the output of the previous calculation being fed back to the network at an intermediate level between its highest (input) level and its lowest (output) level.

**Declaration under Rule 4.17:**

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